Space Time Tradeoff

Is it that Simple?

Space Time Tradeoff

Is it that Simple?
or
What I've been up to and why I haven't done a JUG talk for ages

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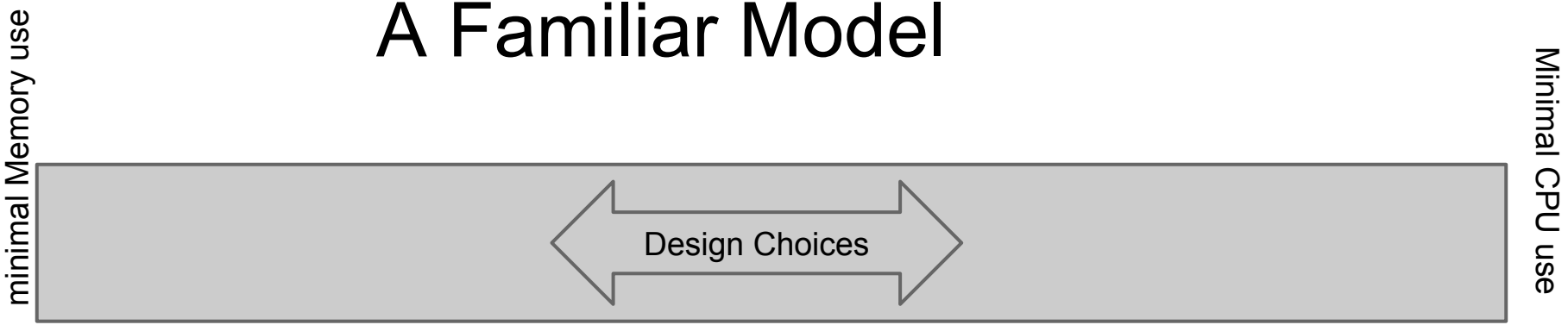
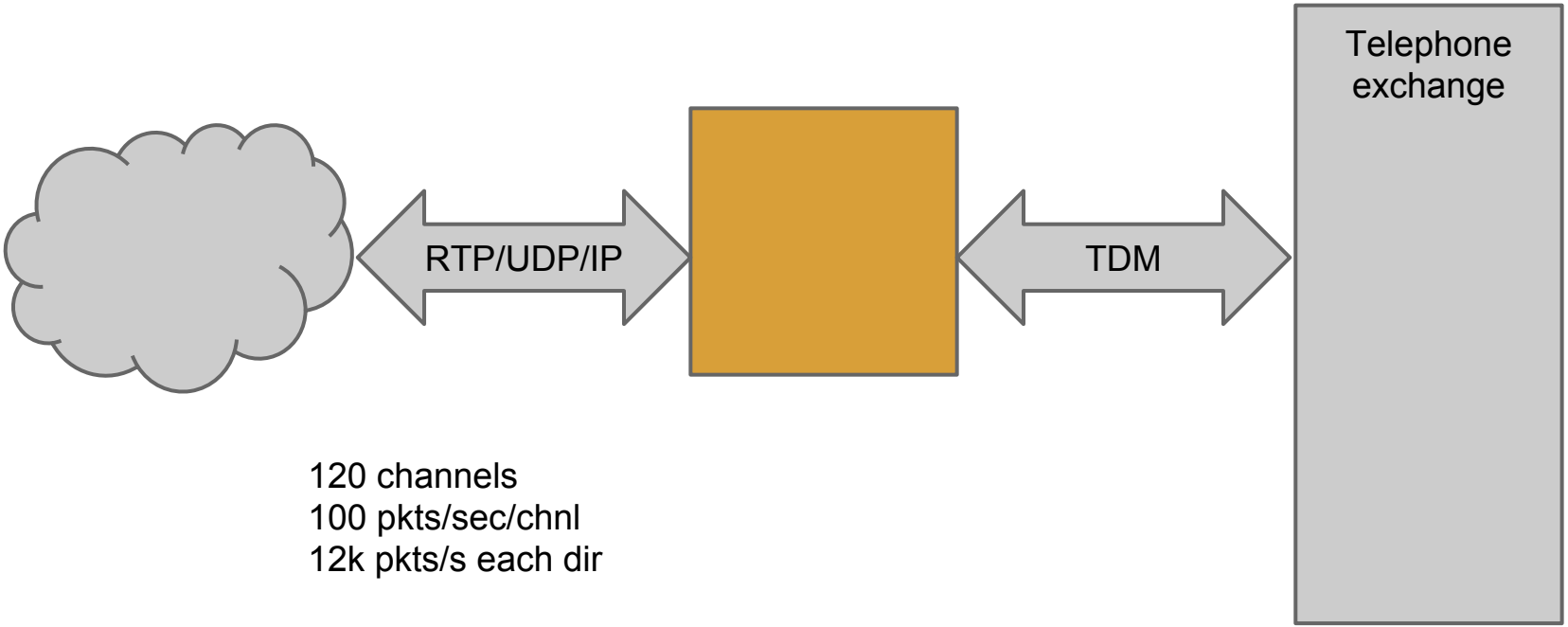
Available for employment / contract from Mid April 2015!

A Familiar Model

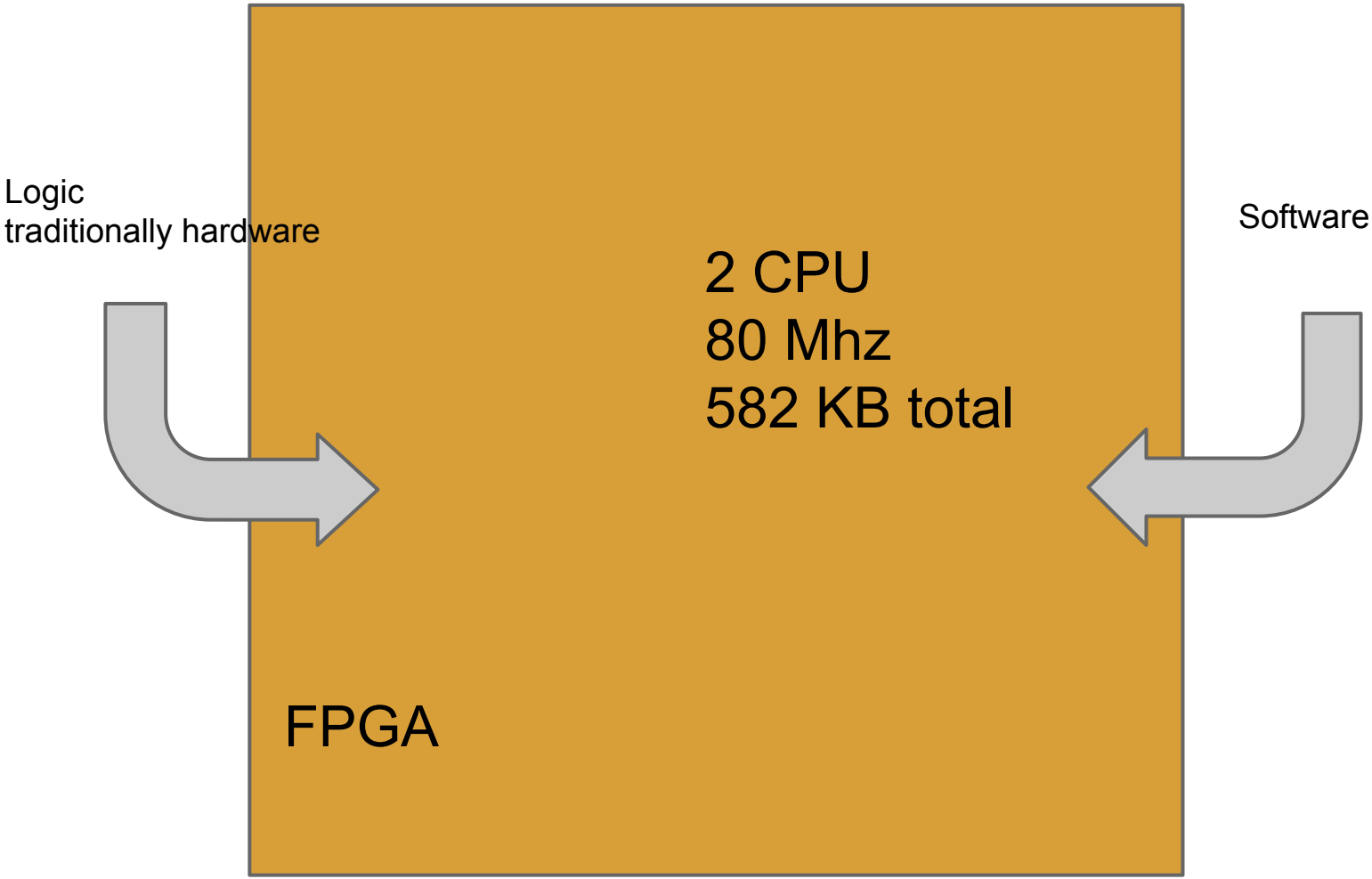


What I've been up to

PSTN / VoIP Gateway



120 channels
100 pkts/sec/chnl
12k pkts/s each dir


Logic
traditionally hardware
Software
2 CPU
80 Mhz
582 KB total
FPGA

What is an FPGA?

Field Programmable Gate Array

ie Programmable Silicon

Logic elements - each containing

- programmable and/or/xor gates (implemented as an LUT)
- 1 bit adder (bypassable)
- 1 register (bypassable)

Ram blocks

Configurable connections / wiring

Some specialist stuff

I felt like I was backed into a corner, with almost no spare CPU or RAM, and yet I was still able to make progress - it was like the walls kept moving back on me.

A Repeating Thought Pattern

Example:

I index through every element of this array, and only do something on the ones that are enabled.

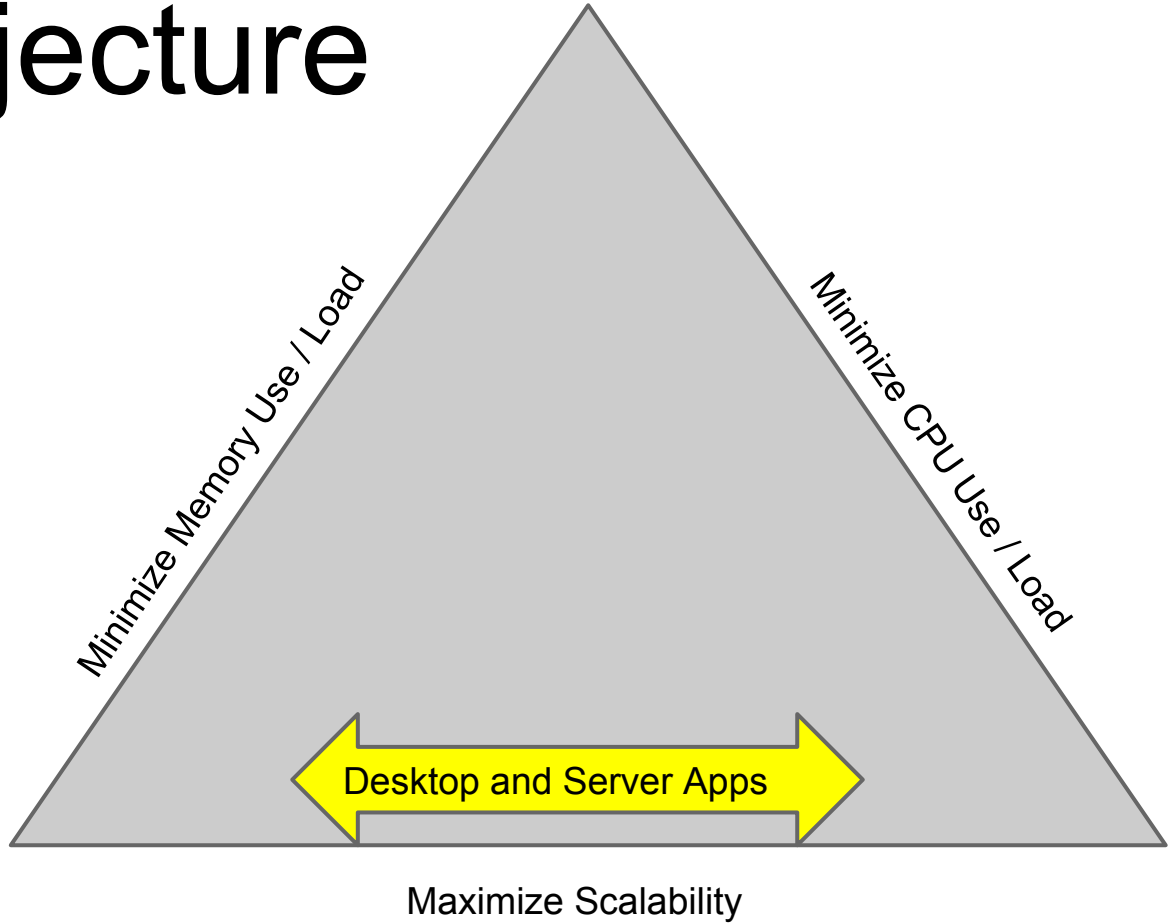
Why don’t I make a linked list of the enabled one, and just traverse the linked list?

That would be much faster when there are only a few enabled.

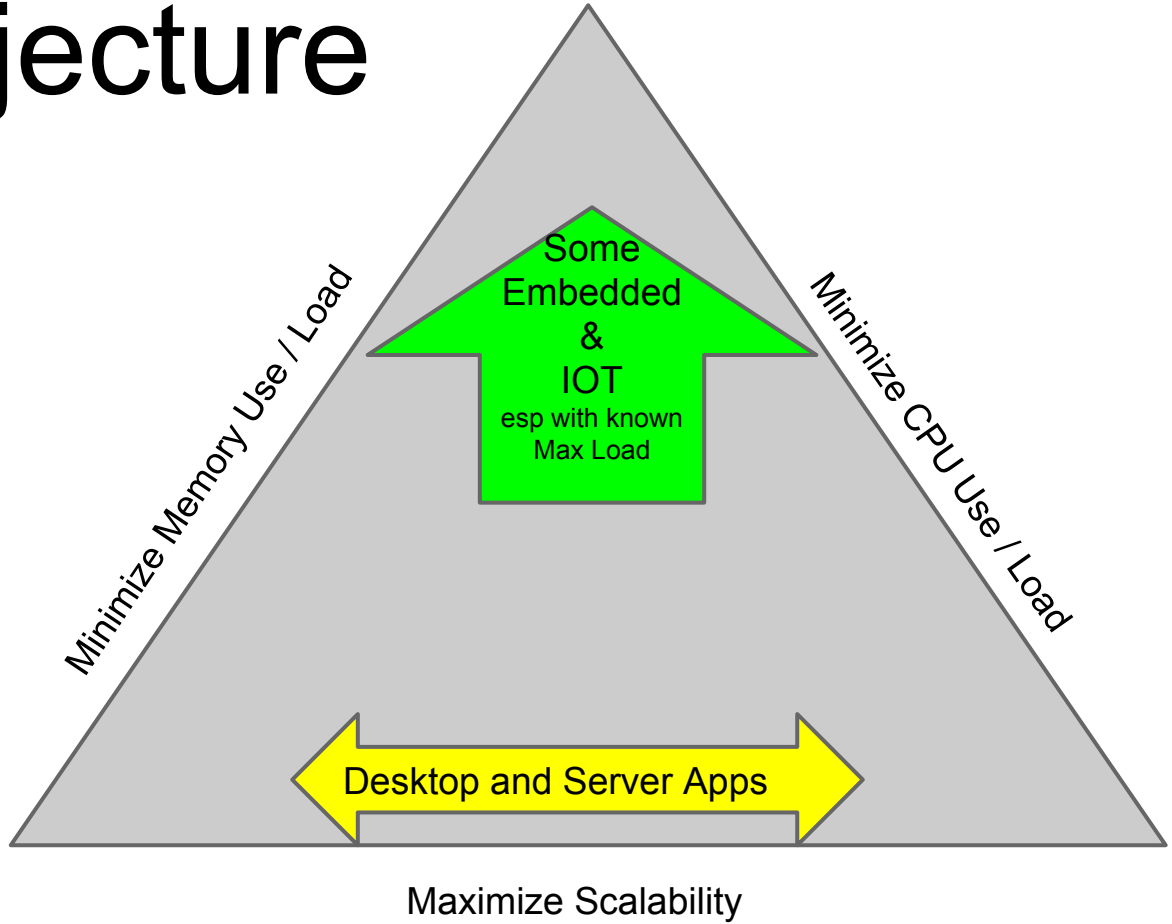
The Key Idea I Kept Forgetting

- The design choice only has to minimize CPU and Memory under the **known Maximum load**
- If it works under maximum load, it will work under light load
- There is no benefit to using less memory under light load
- There is no benefit to using less CPU under light load

Conjecture


Minimize Memory Use / Load
Minimize CPU Use / Load
Desktop and Server Apps
Maximize Scalability

Conjecture


Some
Embedded
&
IOT
esp with known
Max Load
Minimize Memory Use / Load
Minimize CPU Use / Load
Desktop and Server Apps
Maximize Scalability

What is an FPGA?